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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,795	12/21/2005	Kiyoshi Kamiya	XA-10493	5851

181 7590 04/27/2009

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EXAMINER	
LO, KENNETH M	

ART UNIT	PAPER NUMBER
2189	

NOTIFICATION DATE	DELIVERY MODE
04/27/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/561,795	KAMIYA ET AL.	
	Examiner	Art Unit	
	KENNETH M. LO	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2008 and 18 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-11, 18-19 are pending in the Application.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/22/2008 with RCE filed 02/18/2009 has been entered.

Response to Amendment

3. The Amendments as follows are accepted:

Amendment to the claims has been accepted for examination as per amendment received 12/22/2008.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-11 and 18-19** are rejected under 35 U.S.C. 102(b) as being unpatentable over Kaneda et al. [hereinafter Kaneda] (JP 2003-216506).

As per Claim 1, Kaneda discloses, "a rewritable nonvolatile memory" as **["semi-conductor flash memory" (Paragraph 0002)]** "and a control circuit" **["control circuit section " (Paragraph 0008)]** "wherein the rewritable nonvolatile memory includes a plurality of memory cells arranged in a memory array" **["this approach is an approach of changing the field which writes in data, only when modification is added to the read data, and when not adding modification to data at all only by reading data, the count of writing of the field where that data is memorized is still 1 time written in first, and will not use all the fields of a flash memory effectively." (Paragraph 0005) It is inherent that flash memory is structured as an array of memory cells.]** "wherein the memory apparatus brings logical addresses into correspondence with physical addresses of the rewritable nonvolatile memory, and retains a piece of number-of-rewrites information for each logical address" **["The address translation table the control circuit section has remembered conversion of the logical address and the physical address for every block unit of a flash memory to be, It is a thing possessing RAM in which the count table of writing which has memorized the**

counts of writing for every block unit including OS field was prepared. OS field block is rearranged to a free area by the read-out write request of a data area block, said data area block is written in OS field block before rewriting and relocation, and it is characterized by changing an address translation table." (Paragraph 0008)] "wherein a memory cell associated with each logical address includes a piece of data," **["The address translation table the control circuit section has remembered conversion of the logical address and the physical address for every block unit of a flash memory to be, It is a thing possessing RAM in which the count table of writing which has memorized the counts of writing for every block unit including OS field was prepared." (Paragraph 0008)]** "wherein the control circuit can perform replacement of the piece of data in the rewriteable nonvolatile memory, wherein the replacement process is a process of replacing a first physical address corresponding to a given logical address judged to have a small number of rewrites based on the associated piece of number-of-rewrites information with a second physical address so as to bring the given logical address into correspondence with the second physical address and performing data transfer according to the replacement" **["It is a thing possessing RAM in which the count table of writing which has memorized the counts of writing for every block unit including OS field was prepared. OS field block is rearranged to a free area by the read-out write request of a data area block, said data area block is written in OS field block before rewriting and relocation, and it is characterized by changing an address translation table. Moreover, a calculating machine rearranges OS field block to a**

free area by the read-out write request of the data area block from a host, writes said data area block in OS field block before rewriting and relocation, and is characterized by changing an address translation table" (Paragraph 0008 and 0009)].

As per Claim 2, Kaneda discloses "wherein the second physical address is a free physical address used for a correspondence with no logical address" as **["OS field block is rearranged to a free area by the read-out write request of a data area block" (Paragraph 0008)].**

As per Claim 3, Kaneda discloses "wherein the second physical address is a physical address corresponding to a second logical address of the logical addresses, having a larger number of rewrites in comparison to the given logical address having the small number of rewrites," as **["At step 501, it writes in with reference to the count table of writing of the block in a flash memory, and a count is checked. With this check, it writes in at step 502 and existence of the block with many counts, existence of the block currently written in more than the count to which the count of writing was set, etc. are judged, and when there is no block with many counts of writing applicable to these, processing is ended. When there is a block with many counts of writing, it writes in at step 503, and the block with few [the minimum or] counts is selected," (Paragraph 0025)]** "wherein the second logical address is changed so as to be brought into correspondence with the first physical

address to which the given logical address having the small number of rewrites was assigned" **["and it writes in at step 504, and writes in with the block with many counts, and exchange processing with the block with few [the minimum or] counts is performed. Then, the block of an exchange place is copied to RAM206 at step 505, and a flag is set up to the block of a changing agency, and the block of an exchange place at step 506. Exchange processing of the block in a flash memory is carried out at step 507, an address translation table is rewritten at step 508, it changes at step 509, and a flag is cleared." (Paragraph 0025)].**

As per Claim 4, Kaneda discloses, "wherein the replacement process can be performed concurrently with a process in response to a direction for writing provided from an outside of a memory card" as **["Even if the 2nd object of this invention has access from a host at the time of the data exchange in a flash memory, it is to offer the storage and the computer which can replace a data area" (Paragraph 0007)]**

As per Claim 5, Kaneda discloses, "wherein the replacement process can be performed when the number of rewrites of the logical address targeted for the process in response to the direction for writing reaches a given number of times" as **["and OS field before relocation is used as a data area, and the count of writing of the whole field of a flash memory is written in and it brings close to the count of a limitation, in this example, reinforcement is in drawing, using the whole flash memory effectively. In the condition 2, when the data of a data area (1) are read**

and a write request occurs, it replaces by relocating the data of OS field (1) to a free area, and data are written in by making OS field before relocation (1) into a data area (1). As a result of this relocation, as shown in a condition 3, the count of writing of a data area (1) and a free area is set to 2 and 10, respectively. By repeating this processing, near of the count of writing of the whole flash memory can be carried out to the same count," (Paragraph 0018 and 0019)].

As per Claim 6, Kaneda discloses, "wherein the replacement process can be performed on a logical address having a smallest number of rewrites, of arbitrarily extracted logical addresses" as **["In the condition 2, when the data of a data area (1) are read and a write request occurs, it replaces by relocating the data of OS field (1) to a free area, and data are written in by making OS field before relocation (1) into a data area (1). As a result of this relocation, as shown in a condition 3, the count of writing of a data area (1) and a free area is set to 2 and 10, respectively. By repeating this processing, near of the count of writing of the whole flash memory can be carried out to the same count, and it can bring close to the count of a write-in limitation. At this time, conversion of the logical address by having rearranged and a physical address is performed, and that result is memorized to an address translation table. Moreover, when it distinguishes whether the count which the count of writing of this block wrote in and was set up with reference to the count table is become when the data of a data area (1) are read and a write request occurs and the set-up count is become about it, you may make it**

rearrange. By doing in this way, the frequency of relocation decreases and a rewriting rate can be gathered. (Paragraph 0019 and 0020)].

As per Claim 7, Kaneda discloses, "wherein during the process in response to the direction for writing, the control circuit brings a logical address targeted for the process into correspondence with a third physical address and performs data rewrite" as **["the rewriting frequency of each rewriting block is measured, each sector of the block judged that rewriting frequency is high is moved to another specific block, namely, the management method move a logic storing block to the physical block of an expansion field is indicated by by carrying out counting of the count of elimination of the block which stored four sector data, and recording it." (Paragraph 0004)].**

As per Claim 8, Kaneda discloses, "wherein the rewritable nonvolatile memory has an address translation table in which correspondences of the logical addresses and physical addresses are defined" as **["The address translation table the control circuit section has remembered conversion of the logical address and the physical address for every block unit of a flash memory to be," (Paragraph 0008)].**

As per Claim 9, Kaneda discloses, "wherein the piece of number-of-rewrites information for each logical address is retained in a region of the physical address corresponding to the logical address" **["Moreover, since RAM is volatile memory, if**

feed is no longer performed by the power off of a system, as for the management information in the translation table 207 of RAM206 of the control circuit section 202, the count table 208 of writing, and the exchange condition table 209, data will disappear. in order to avoid this -- the inside of the control circuit section 202 -- the power off judging change circuit 205 -- **** from a system -- **** -- things are distinguished, the feed to the control circuit section 202 and a flash memory is changed to a dc-battery 203, and the data in RAM206 are evacuated to a flash memory." (Paragraph 0022) "the managed table of RAM206 in the control circuit section 202, and each condition of a condition 1 to the condition 3 is equivalent to each condition shown in drawing 3 . A managed table consists of an address translation table, data semantics, a count table of writing, and an exchange condition table." (Paragraph 0023)].**

As per Claim 10, Kaneda discloses, "wherein the piece of number-of-rewrites information for each logical address is retained in a number-of-rewrites table" as **["It is a thing possessing RAM in which the count table of writing which has memorized the counts of writing for every block unit including OS field was prepared" (Paragraph 0008)].**

As per Claim 11, Kaneda discloses, "a rewritable nonvolatile memory" as **["semi-conductor flash memory" (Paragraph 0002)]** "and a control circuit" **["control circuit section " (Paragraph 0008)]** "wherein the rewritable nonvolatile memory

includes a plurality of memory cells transistors arranged in a memory array" **["this approach is an approach of changing the field which writes in data, only when modification is added to the read data, and when not adding modification to data at all only by reading data, the count of writing of the field where that data is memorized is still 1 time written in first, and will not use all the fields of a flash memory effectively." (Paragraph 0005) It is inherent that flash memory is structured as an array of memory cells. It is also inherent that memory cells are made of transistors.]** "wherein the memory card brings logical addresses into correspondence with physical addresses of the rewritable nonvolatile memory, and retains a piece of number-of-rewrites information for each logical address" **["The address translation table the control circuit section has remembered conversion of the logical address and the physical address for every block unit of a flash memory to be, It is a thing possessing RAM in which the count table of writing which has memorized the counts of writing for every block unit including OS field was prepared. OS field block is rearranged to a free area by the read-out write request of a data area block, said data area block is written in OS field block before rewriting and relocation, and it is characterized by changing an address translation table." (Paragraph 0008)]** "wherein a memory cell transistor associated with each logical address has a piece of data," **["The address translation table the control circuit section has remembered conversion of the logical address and the physical address for every block unit of a flash memory to be, It is a thing possessing RAM in which the count table of writing which has memorized the**

counts of writing for every block unit including OS field was prepared." (Paragraph 0008)] "wherein the control circuit can execute are write process of the rewritable nonvolatile memory in response to a direction for writing from an outside, and a replacement process of the piece of data on the nonvolatile memory" **["writes said data area block in OS field block" (Paragraph 0009) It is inherent that the control block can write the memory.]** "wherein the replacement process is a process of replacing a first physical address corresponding to a given logical address judged to have a small number of rewrites based on the associated piece of number-of-rewrites information with a second physical address so as to bring the given logical address into correspondence with the second physical address and performing data transfer according to the replacement" **["It is a thing possessing RAM in which the count table of writing which has memorized the counts of writing for every block unit including OS field was prepared. OS field block is rearranged to a free area by the read-out write request of a data area block, said data area block is written in OS field block before rewriting and relocation, and it is characterized by changing an address translation table. Moreover, a calculating machine rearranges OS field block to a free area by the read-out write request of the data area block from a host, writes said data area block in OS field block before rewriting and relocation, and is characterized by changing an address translation table" (Paragraph 0008 and 0009)].**

As per Claim 18, Kaneda discloses, "wherein the memory array has a plurality of word lines and a plurality of bit lines connected to the memory cells" **["semi-conductor flash memory" (Paragraph 0002) Flash memory is inherently arranged with a plurality of word lines and bit lines to access an array of memory cells.]** "wherein a memory cell targeted for rewrite shares a word line or a bit line with a memory cell not targeted for rewrite" **["However, this approach is an approach of changing the field which writes in data, only when modification is added to the read data, and when not adding modification to data at all only by reading data, the count of writing of the field where that data is memorized is still 1 time written in first, and will not use all the fields of a flash memory effectively." (Paragraph 0005)]**

As per Claim 19, Kaneda discloses, "wherein the memory array has a plurality of word lines and a plurality of bit lines connected to the memory cells" **["semi-conductor flash memory" (Paragraph 0002) Flash memory is inherently arranged with a plurality of word lines and bit lines to access an array of memory cells.]** "wherein a memory cell targeted for rewrite shares a word line or a bit line with a memory cell not targeted for rewrite" **["However, this approach is an approach of changing the field which writes in data, only when modification is added to the read data, and when not adding modification to data at all only by reading data, the count of writing of the field where that data is memorized is still 1 time written in first, and will not use all the fields of a flash memory effectively." (Paragraph 0005)].**

Response to Arguments

4. Applicant's arguments filed have been fully considered but they are not persuasive.

Applicant argues:

(a) "Specifically, in contrast to Applicants' invention, Kaneda does not teach or suggest a memory cell associated with each logical address including a piece of data." Page 7.

With respect to (a), Examiner appreciates the interpretative description given by Applicant in response. As shown in Fig 4, as Applicant pointed out, shows address 4 referencing physical address 0, and it being marked as Empty or Free region. However, each memory cell associated with each logical address still includes a piece of data, that data being data that indicates the region is empty or free. It is inherently known in the art of memory cells that regardless of whether data in a memory cell is considered valid or not, even "erased" or "empty" memory cells contain data of the erased state. For example, an erased NOR flash cell is a cell reset to the "1" state.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENNETH M. LO whose telephone number is (571)272-9774. The examiner can normally be reached on Mon - Thu (7:30am - 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bragdon Reginald can be reached on 571-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S. Sough/
Supervisory Patent Examiner, Art Unit 2188
04/23/09

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